## REMARKS

A new Action was requested March 18, 2003, but the new Action has not yet issued and extensions would become due if it does not. Therefore, in an effort to advance prosecution while waiting for the new Action or avoid higher extension fees if the new Action that is still requested to eliminate the extension fees does not issue.

The references cited against Claim 1 under 35 USC§103 (a) were based on Buckingham et al. (U.S. Pat. No. 5,345,449, which is most conformity with the description in the action, but not U.S. Pat. No. 6,515,519), in view of Tsern et al. (U.S. Pat. No. 6,263,448). However, there are a number of substantial differences between the present invention and the Buckingham and Tsern et al.'s patents.

(1) According to the abstract, summary (Col. 2, lines 1-15) and FIGS. 1-4 of the Buckingham et al. patent, it mainly provides an integrated circuit comprising: a multiplexer (numeral 2 in FIG. 1) for receiving input data at a normal clock rate (25MHz in FIG. 1). The incoming data latched by a low rate clock signal is multiplexed into a high rate data stream to be passed to a high-speed device (numeral 4 in FIG. 1). The operations of the multiplexer 2 and the high-speed device 4 are controlled by an on-chip clock accelerator 6, which receives the low rate clock signal and generates therefrom a high rate clock signal CLK. The signal CLK comprises two signals in antiphase, CLK1 and CLK2.

The Buckingham et al. patent did not include any low rate region (25MHz is only a normal clock input, specifically, as same as the oscillator of the present invention). In fact, the object is to generate high rate clocks via a low rate clock input, so the Buckingham et al. patent is different from the present invention.

(2) According to the abstract of the Tsern et al. patent, it discloses a memory device with multiple clock domains. However, by the way that separate clocks to different portions of the control circuitry create different clock domains. As shown in FIG. 8, a memory 140 has a slow clock input circuit 144 (low frequency clock region), which includes only one DLL or PLL 150 for generating low frequency clocks. However, the slow clock input circuit 144 does not include any DLL or PLL for increasing a number of the high frequency clocks. Another DLL or PLL 150 belongs to the fast clock input circuit 146, not to the slow clock input circuit 144. In other words, only one slow PLL/DLL (144) or fast PLL/DLL (146) is selected by the fast/slow signal (152) at one time to be used for clock source.

In contrast, the present invention discloses one PLL (33) for low-frequency I/O clock source, and one clock source (35) for high-frequency CPU/SDRAM clock source, and a number of DLL for skew cancellation between CPU/SDRAM clock source (35) and AGP/PCI clock source (34). The PLLs and DLLs work non-stop to use as the different clock sources, not only using one or two output of PLL/DLL at one time. As a result, the Tsern et al. patent is just a practice form of the prior art disclosed in FIG. 2 of the application.

(3) As stated above, the Buckingham et al patent does not disclose a universal clock generator like the present invention, even in view of the Tsern et al.'s patents. In fact, the clock generators taught by them are more similar to the prior art of the present invention.

With respect to Claims 3, 4 and 15, the examiner rejected them based on the ground of Claim 1. However, since Claim 1 has novelty and non-obviousness, then Claims 3, 4 and 15 have novelty and non-obviousness as well.

Reconsideration and allowance are, therefore, requested.

Respectfully submitted,

William R. Evans
c/o Ladas & Parry LLP
26 West 61st Street
New York, New York
Reg. No. 25858
Tel. No. (212) 708-1930